Low Power Reconfigurable FPGA Transponder

Completed Technology Project (2013 - 2017)

Project Introduction

This task will develop a prototype flight transponder based on low power FPGAs capable of implementing existing Electra, CoNNECT, UST, and Iris waveforms.

Under this initiative, a prototype Ka-Band exciter and receiver are under development; suitable FPGAs that are lower power than the Virtex 5 but still compatible with a deep space environment are being surveyed with a goal of a lower power Iris V2 implementation; and a trade study is being conducted to determine under what conditions a CPU is needed and what software would run on it.

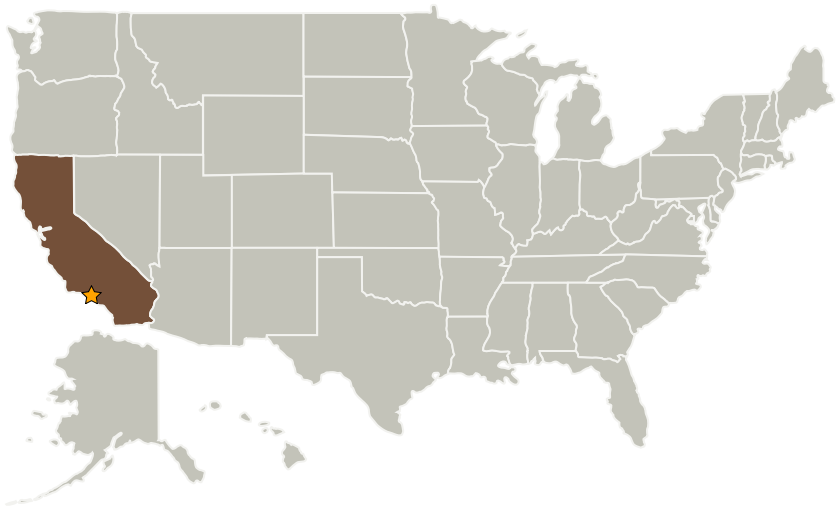
Anticipated Benefits

Increased science return

Increased competitiveness and data return for smallsats

Increased data return for smallsats

Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
★Jet Propulsion Laboratory(JPL)	Lead Organization	NASA Center	Pasadena, California

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Table of Contents

Organizational Responsibility

Responsible Mission Directorate:

Mission Support Directorate (MSD)

Lead Center / Facility:

Jet Propulsion Laboratory (JPL)

Responsible Program:

Center Independent Research & Development: JPL IRAD

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Primary U.S. Work Locations
California

Project Management

Program Manager:

Fred Y Hadaegh

Project Manager:

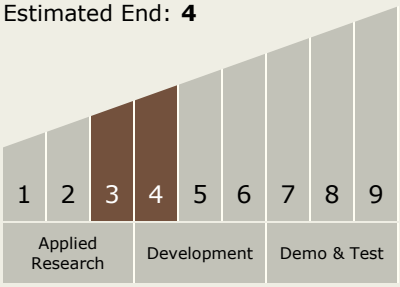
Jonas Zmuidzinas

Principal Investigator:

Courtney B Duncan

Technology Maturity (TRL)

Start: **3**
Estimated End: **4**



Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.5 High Performance Field Programmable Gate Arrays